



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,288	11/13/2003	Kazuaki Kurihara	032104	5663
38834	7590	09/19/2005	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			HA, NGUYEN T	
			ART UNIT	PAPER NUMBER
			2831	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/706,288

Applicant(s)

KURIHARA ET AL.

Examiner

Nguyen T Ha

Art Unit

2831

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) 11-25 and 29-37 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4-10 and 26-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendment filed on 7/11/2005 has been entered and acknowledged by the examiner.

Response to Arguments

2. Applicant's arguments with respect to claims 1-2, 4-10 and 26-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2, 4-10 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Block et al. (US 6,737,728) in view of Jeon et al. (US 6,753,221).

Regarding claim 1, Block et al. disclose a thin layer element comprising a capacitor with a dielectric layer (258) made of a metal oxide, and at least one protective insulating layer/ILD (266) made of a cured resin, in which a barrier layer (264) comprising a non-conductive inorganic material (silicon nitride, column 7, lines 39-40) being provided between the capacitor and the protective insulating layer/ILD (figure 12).

Block et al. lack the barrier layer is a material having the same thermal expansion coefficient as that of the dielectric layer.

Jeon et al. teach a barrier layer and a dielectric comprising TiO_2 (column 4, lines 19-21, and lines 45-46). (Examiner noted that the barrier layer and dielectric layer of Jeon et al. having the same thermal expansion coefficient, since they both made of the same materials).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the dielectric and barrier layers as taught by Jeon et al. in Block et al., in order to avoid problems interlayer peeling and high reliability for the capacitor.

Regarding claim 2, Block et al. disclose a thin layer capacitor element comprising a substrate (252) having formed thereon a capacitor with a dielectric layer (158) made of a metal oxide (tantalum oxide, column 7, lines 5-6), in which a barrier layer (264) comprising a non conductive inorganic material (silicon nitride, column 7, lines 39-40) being covering at least the top and side of the capacitor (figure 12), and at least one

protective insulating layer/ILD (266) made of a cured resin is formed on the barrier layer.

Block et al. lack the barrier layer is a material having the same thermal expansion coefficient as that of the dielectric layer.

Jeon et al. teach a barrier layer and a dielectric comprising TiO_2 (column 4, lines 19-21, and lines 45-46). (Examiner noted that the barrier layer and dielectric layer of Jeon et al. having the same thermal expansion coefficient, since they both made of the same materials).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the dielectric and barrier layers as taught by Jeon et al. in Block et al., in order to avoid problems interlayer peeling and high reliability for the capacitor.

Regarding claim 4, the teaching of Block et al. in view of Kirlin includes the barrier layer has the same composition as that of the dielectric layer (Kirlin disclose column 5, lines 19-21 and Block disclose column 7, lines 5-6).

Regarding claim 5, Block et al. disclose the barrier layer (264) is silicon nitride (column 7 lines 40-41).

Regarding claim 6, Block et al. disclose the barrier layer is amorphous (figure 12).

Regarding claim 7, Block et al. disclose the dielectric layer comprises a composite metal oxide comprising at least one metal selected from tantalum (Ta) (column 7, lines 5-6).

Regarding claim 8, Block et al. further disclose the terminals (101 & 102) for external electrical connection provided at least at a location other than the edge of one side of the package (figure 1).

Regarding claim 9, Block et al. disclose a plurality of capacitors with different capacitances are provided in one thin layer capacitor element (figure 2).

Regarding claim 10, Block et al. disclose the capacitor is formed on the substrate (not shown) via an adhesion layer (110) having the same material composition as that of the barrier layer (figure 1).

Regarding claim 26, the method steps are necessitated by the device structure as it is disclosed by Block et al. comprising a capacitor (figure 12) with a dielectric layer made of a metal oxide (tantalum oxide, column 7, lines 5-6) and at least one protective insulating layer/ILD (266) made of a cured resin, which comprises the steps of:

- forming a capacitor (figure 12);
- forming a barrier layer (264), from a non-conductive inorganic material, on the capacitor; and
- forming at least one protective insulating layer (266) on the barrier layer (264) so that the capacitor and the protective insulating layer is separated from the barrier layer.

Block et al. lack the barrier layer is a material having the same thermal expansion coefficient as that of the dielectric layer.

Jeon et al. teach a barrier layer and a dielectric comprising TiO_2 (column 4, lines 19-21, and lines 45-46). (Examiner noted that the barrier layer and dielectric layer of

Art Unit: 2831

Jeon et al. having the same thermal expansion coefficient, since they both made of the same materials).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the dielectric and barrier layers as taught by Jeon et al. in Block et al., in order to avoid problems interlayer peeling and high reliability for the capacitor.

Regarding claim 27, the method steps are necessitated by the device structure as it is disclosed by Block et al. comprising the steps of:

- forming a capacitor with a dielectric layer (158, column 7, lines 5-6), from a metal oxide, on a substrate;
- forming a barrier layer (264), from a non-conductive inorganic material, to cover at least the top and side of the capacitor; and
- forming at least one protective insulating layer/ILD (266), from a cured resin on the barrier layer so that the capacitor and the protective insulating layer is separated from the barrier layer.

Block et al. lack the barrier layer is a material having the same thermal expansion coefficient as that of the dielectric layer.

Jeon et al. teach a barrier layer and a dielectric comprising TiO_2 (column 4, lines 19-21, and lines 45-46). (Examiner noted that the barrier layer and dielectric layer of Jeon et al. having the same thermal expansion coefficient, since they both made of the same materials).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the dielectric and barrier layers as taught by Jeon et al. in Block et al., in order to avoid problems interlayer peeling and high reliability for the capacitor.

Regarding claim 28, Block et al. further comprises the step of forming the dielectric layer by a sputtering method/etching (column 11, lines 24-25).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

Art Unit: 2831

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Nguyen T. Ha'. The signature is fluid and cursive, with a large initial 'N' and a long, sweeping horizontal stroke at the end.

Nguyen T. Ha
September 9, 2005